Notice of Allowability	Application No.	Applicant(s)	
	10/808,402	ISHIKURA ET AL.	
	Examiner	Art Unit	
	Gene N. Auduong	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed March 25, 2004*.

2. ☒ The allowed claim(s) is/are *1-46*.

3. ☒ The drawings filed on *25 March 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3-25-04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Gene N Auduong
Primary Examiner
Art Unit 2827

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on March 25, 2004 is being considered by the examiner.

Allowable Subject Matter

3. Claims 1-46 are allowed.

4. The following is an examiner's statement of reasons for allowance: The prior art does not teach or fairly disclose, in addition with other limitation in the claim, claiming CMOS SRAM cells, being arranged on a semiconductor substrate in a matrix shape, each comprising a pair of access transistors, a pair of drive transistors, and a pair of load transistors, each region being a cell region with an elongated shape in a row direction, wherein three well regions are formed side by side in a row direction so that a second conductivity type well region may be disposed between two first conductivity type well regions on the semiconductor substrate, and wherein one of the access transistors and one of the drive transistors are formed in each of two the first conductivity type well regions within the cell region, and a pair of the load transistors is formed in the second conductivity type well region; and comprising a plurality of interconnection layers over transistors which configure the CMOS SRAM cell; the semiconductor memory device, comprising: a plurality of paired bit lines, formed of one of the plurality of interconnection layers, each being extended in a column direction to be connected to the CMOS SRAM cell in

the same column, and arranged in parallel in a row direction or a plurality of paired bit lines, formed of the interconnection layer upper than that of the word line by one layer, and each being extended in a column direction to be connected to the CMOS SRAM cell in the same column, and arranged in parallel in a row direction; a plurality of high potential side power supply interconnections, formed of the same interconnection layer as that of the bit line, and each being arranged between the paired bit lines to be connected to the CMOS SRAM cell in the same column or a plurality of high potential side power supply interconnections, formed of one of the plurality of interconnection layers, each being extended in a column direction to be connected to the CMOS SRAM cell in the same column, and arranged in parallel in a row direction; a plurality of word lines, formed of the interconnection layer upper than that of the bit line by one layer, each being extended in a row direction to be connected to the CMOS SRAM cell in the same row, and arranged in parallel in a column direction or a plurality of word lines, formed of one of the plurality of interconnection layers, each being extended in a row direction to be connected to the CMOS SRAM cell in the same row, and arranged in parallel in a column direction; and a low potential side power supply interconnection, formed of the interconnection layer upper than that of the word line by one layer, and connected to the CMOS SRAM cell or a low potential side power supply interconnection, formed of the interconnection layer upper than that of the bit line by one layer, and connected to the CMOS SRAM cell.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N. Auduong whose telephone number is (571) 272-1773. The examiner can normally be reached on 9-5-4, alternate second Monday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
March 19, 2005

Gene N Auduong
Primary Examiner
Art Unit 2827